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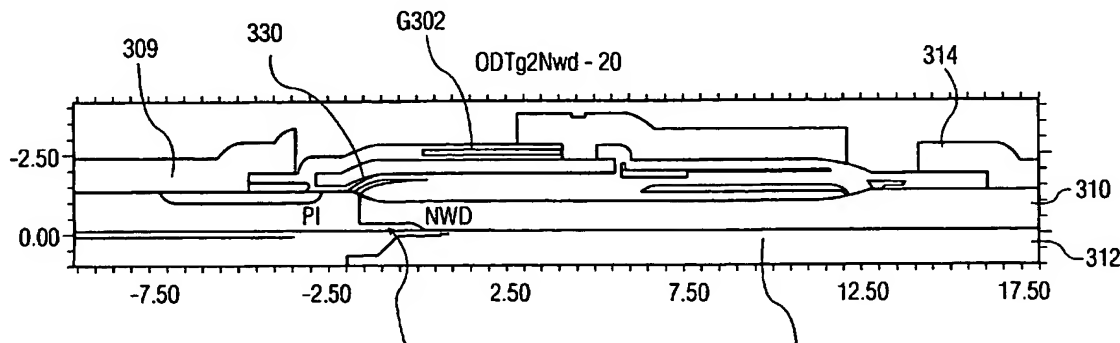
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ning of each regular issue of the PCT Gazette.

(54) Title: **SILICON-ON-INSULATOR DEVICE**



(57) Abstract: A Silicon on Insulator (SOI) device is disclosed wherein an extension of P-type doping (303) is implanted between the buried oxide layer of the device and the SOI layer. The extension is of a size and shape to permit the source (309) to be biased at a voltage significantly less than the handler wafer (304) and drain, a condition under which prior art SOI devices may not properly operate.

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